

TECHNICAL ARTICLE

Enabling Future Innovations—Part 3: 2kW Quarter-Brick Module Reference Design

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Abstract

The increasing reliance on AI, machine learning, and cloud-based applications has driven an unprecedented demand for compact, efficient, and reliable power conversion solutions. This article presents a quarter-brick DC-to-DC converter reference design for legacy data center 48V intermediate bus conversion, offering superior performance compared to existing market alternatives. The design leverages Analog Devices' discrete solution within a common footprint package, delivering a highly competitive and scalable solution to meet the growing requirements of high-performance applications, including hyperscale computing and industrial systems.

Introduction

The quarter-brick module (QBM) reference design is a high-performance DC-to-DC converter based on Analog Devices, Inc.'s (ADI's) quarter-brick (QB) system architecture. It incorporates a new series of coupled inductors to meet strict Distributed-Power Open Standards Alliance (DOSA) dimension requirements while delivering 2kW of continuous power within the constraints of a common footprint package (CFP). With this design approach, the QBM solution reduces the accumulated and traditional power losses from a hard switching converter and enhances operational efficiency, providing a robust solution for demanding applications.

By leveraging ADI's latest 48V/54V to 12V intermediate bus conversion (IBC) technology, the reference design simplifies complexity and enables rapid development cycles for customers. Comprehensive data presented in this article demonstrates measurable improvements in efficiency, thermal performance, and scalability—positioning this solution as a next-generation power module for legacy higher power demand data center environments. Furthermore, its architecture supports current IBC requirements and offers a pathway for future high-voltage systems operating on 400V to 800V bus supplies.

QBM Design

The QBM reference design adheres to the DOSA standard mechanical pinout commonly used in the market, as seen in Figure 1, ensuring seamless integration into existing system boards. When operating as a single module, the pinout can be simplified to include only PMBus® signals. The detailed pin configuration is provided in Table 1.

Table 1. Pin Configuration of ADI's Quarter-Brick Module Reference Design

Pin No.	Pin Name	Function
1	+V _{IN}	Positive input pin
2	RC	DC-to-DC EN
3	-V _{IN}	Negative input pin
4, 5	-V _O	Negative output pin
6	PG	Power good
7, 8	+V _O	Positive output pin
9	SS	Soft start pin
10	CLK_IN	External clock input
11	-VSNS	Negative remote sense output
12	SDA	PMBus data
13	SALERT	PMBus alert
14	SCL	PMBus clock
15	SA1	PMBus ASEL1 address tri-state
16	SA0/+VSNS	PMBus ASEL0 address tri-state/ positive remote sense output
17	ISHARE	Active current-sharing pin

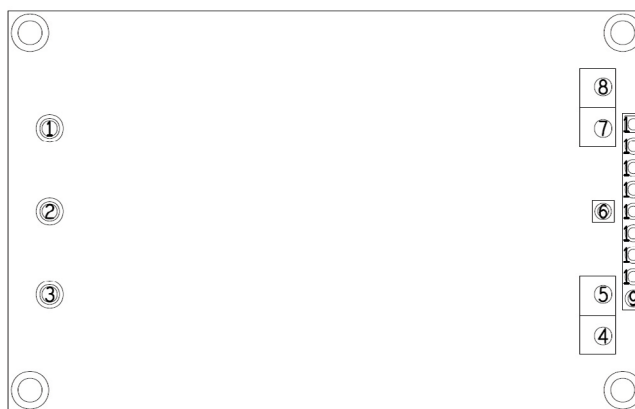


Figure 1. QBM reference pin configuration.

The reference design includes a flat-top baseplate for effective cooling of the power converter FETs, as shown in Figure 2. This baseplate is engineered for optimal thermal management and supports extended power delivery when paired with an off-the-shelf QB heatsink.

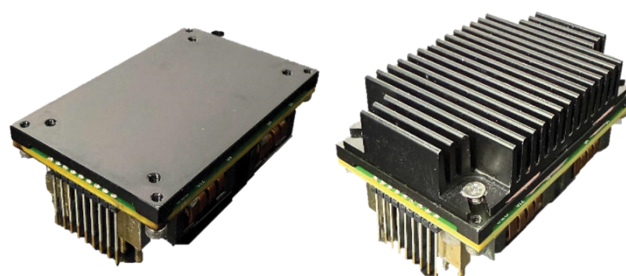


Figure 2. The QBM with flat-top baseplate and with off-the-shelf extended heatsink.

The QBM reference design can be configured using ADI's proprietary, user-friendly [LTpowerPlay](#)® software in conjunction with a DC1613 dongle. This tool enables users to set typical operating parameters, define fault trigger levels and corresponding responses, and log into operational cycles for comprehensive monitoring and control. Figure 3 shows the QBM's user interface in LTpowerPlay.

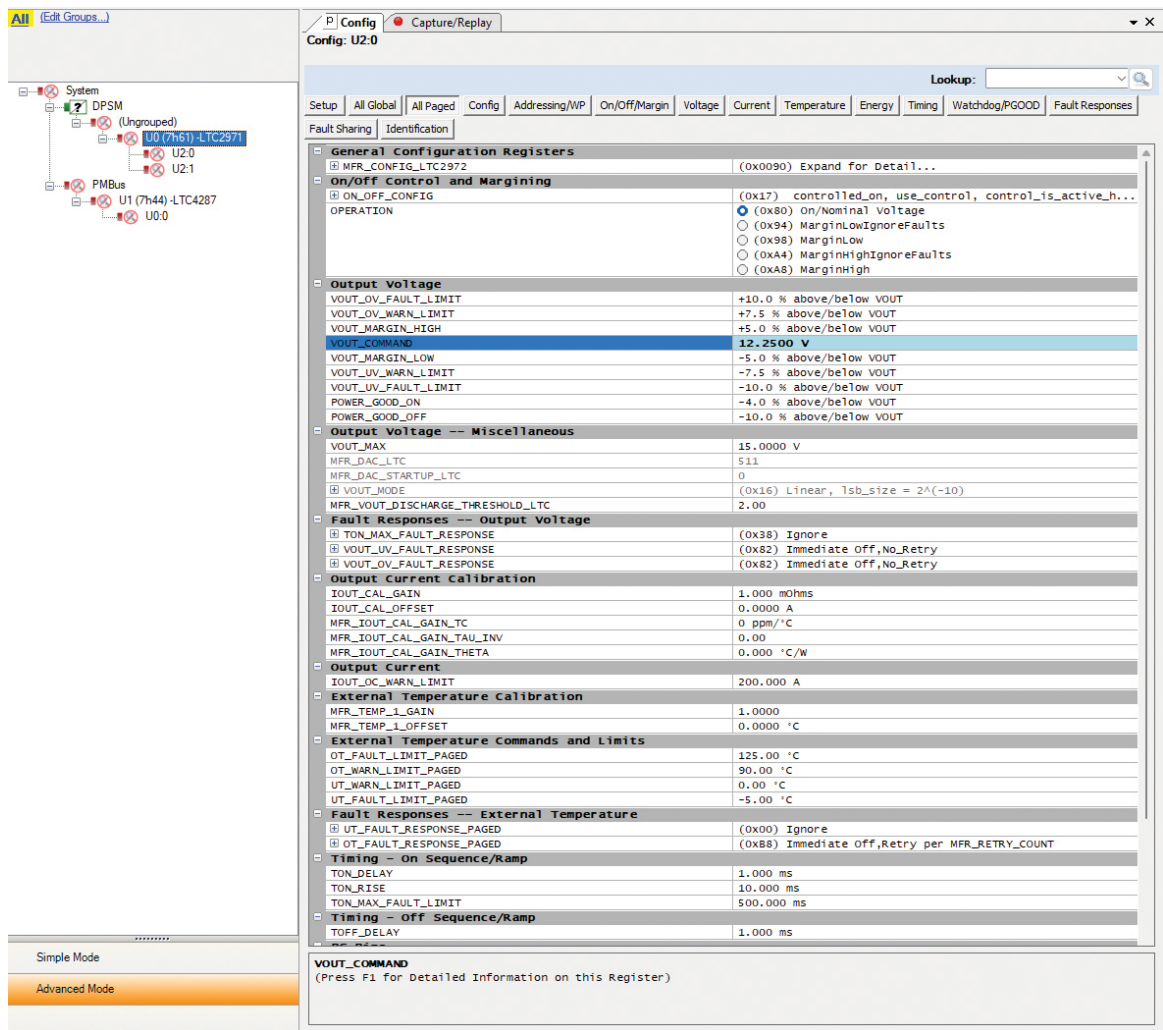


Figure 3. LTpowerPlay configuration GUI to adjust various parameters.

Electrical Performance

This section highlights the key electrical performance metrics that demonstrate the superior capabilities of the ADI QBM reference design compared to existing QBMs on the market. The most critical parameter is efficiency and associated power loss. For accurate evaluation, efficiency measurements are taken before the terminals, ensuring that only the DC-to-DC converter performance is assessed. This approach allows engineers to design custom terminals to further optimize the overall system. Figure 4 shows the efficiency curve from 48V to 60V operation.

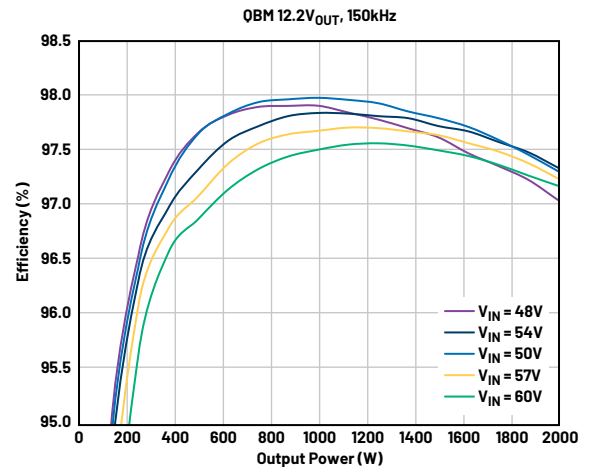


Figure 4. QBM efficiency graph from 48V_{IN} to 60V_{IN}.

This QBM is engineered to achieve exceptional efficiency, delivering over 97% at full load and reaching a peak of 98%. Such performance significantly reduces power losses and improves thermal management, minimizing cooling requirements across data center operations. Additionally, the design is optimized for 50V operation, positioning it as an ideal downstream converter for future high-voltage (HV) data center architectures, including 800V systems utilizing a 16:1 conversion ratio.

Thermal Performance

Thermal performance is a critical indicator for high-power-density solutions. While the converter can technically support large power outputs, its capability is ultimately constrained by the thermal design power within its intended volume. The QBM reference design demonstrates that even in space-limited environments, it can deliver its rated output power without triggering an overtemperature shutdown.

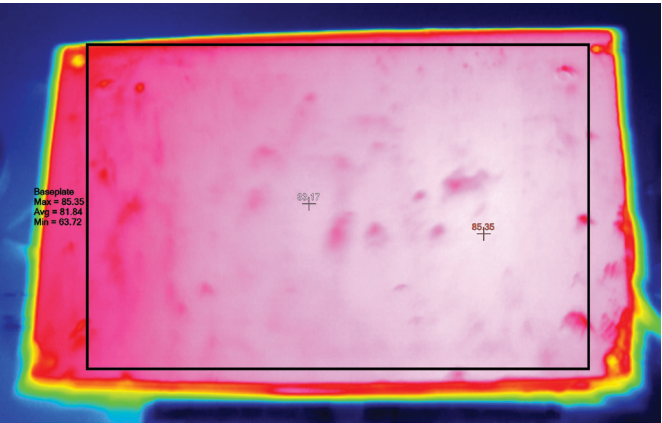


Figure 5. Thermal capture of 48VIN at 25°C ambient temperature.

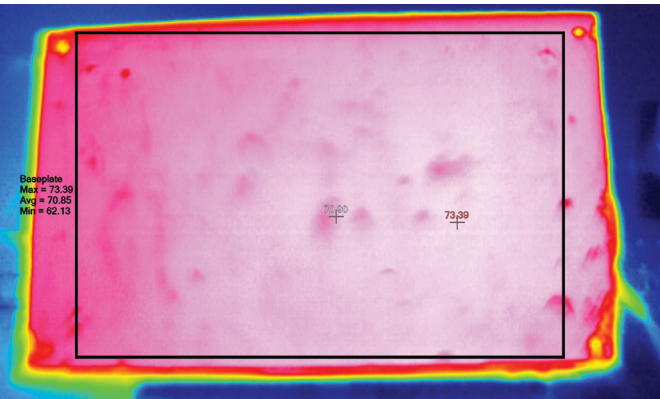


Figure 6. Thermal capture of 54VIN at 25°C ambient temperature.

Thermal images for both 48V and 54V operation are shown in Figure 5 and Figure 6, respectively. The results indicate a well-distributed temperature across its flat-baseplate surface (without extended heatsink), with only minimal deviation from the hotspot. This demonstrates that good positioning of critical components and effective copper layout design minimizes thermal concentration, ensuring reliable operation without thermal limitations.

Fault Response

The QBM reference design integrates the [LTC2971](#) as its power management controller, supporting PMBus Level 1 compliance. This controller monitors key parameters such as voltage, current, and temperature, and initiates appropriate fault responses. Users can configure the module to either latch or retry upon specific fault conditions, providing flexibility and robust system protection.

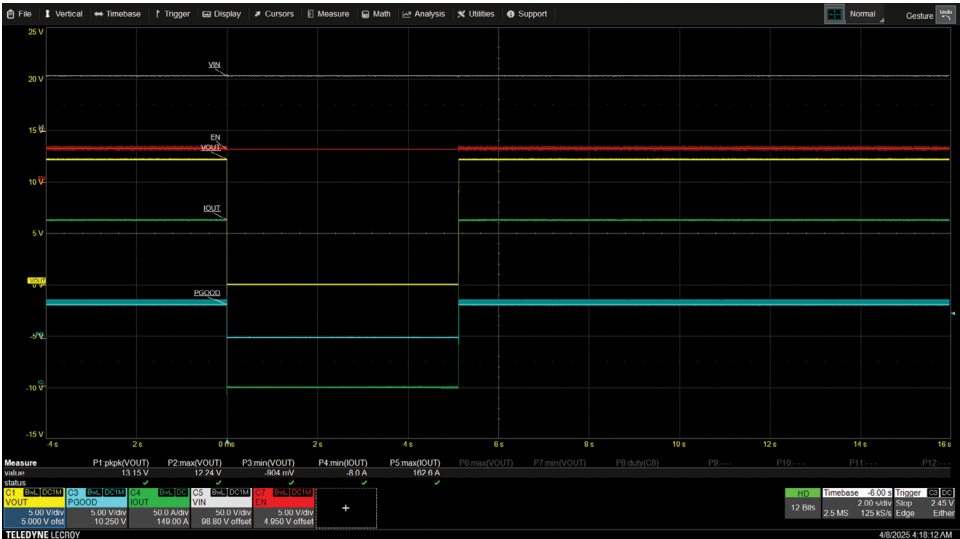


Figure 7. The QBM shuts down for 5s after hitting the OTP level.

The airflow for this evaluation is from the right side of the picture going to the left. The test setup is also evaluated without the baseplate to profile the hotspot per power stage inside the module as seen in Figure 10.

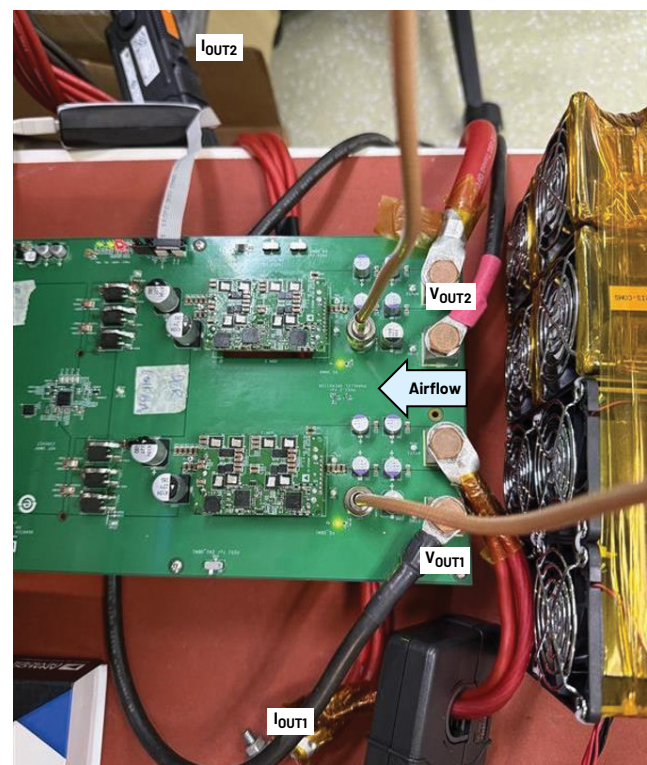


Figure 10. Test setup of two QBMs operating in parallel.

The measure of performance for parallel operation is the amount of current mismatch the modules have. Figure 11 shows the reading of two modules operating at 4kW combined. The lower the current mismatch, the better the current sharing. This is also

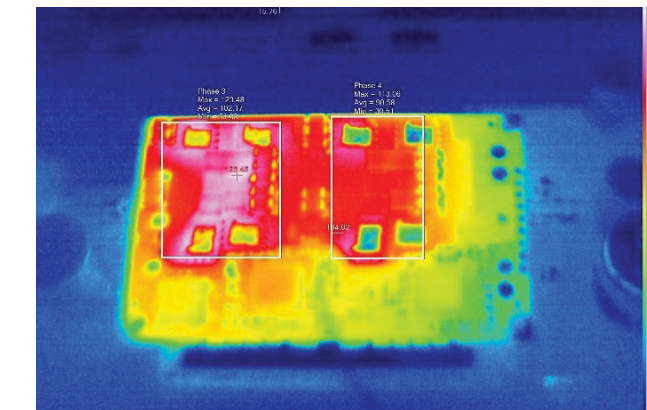


Figure 13. Thermal shots of two QBMs operating in parallel.

important to ensure that the modules are operating at the same thermal condition, thereby maximizing both modules’ power output handling capabilities. Figure 12 shows the current mismatch performance for this setup.

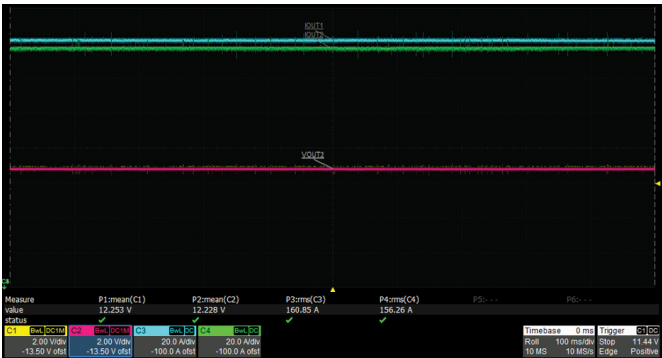


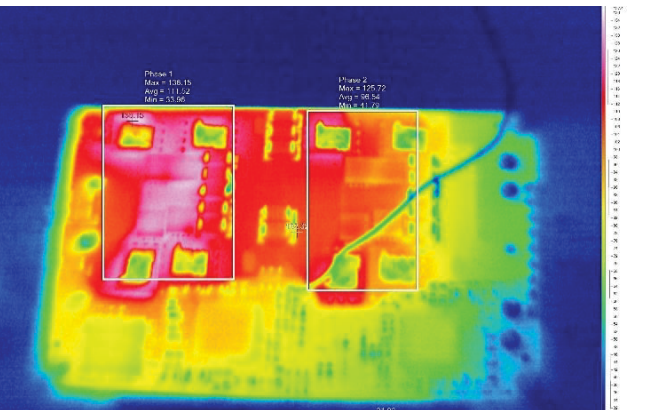
Figure 11. Two QBMs operating at 4kW with 4A current difference.

Iload	Mod1 Current	Mod2 Current	Delta	% error
180	91.45	85.22	6.23	3.53
220	110.93	105.63	5.3	2.45
260	130.62	125.65	4.97	1.94
300	152.26	145.47	6.79	2.28
320	161.15	155.7	5.45	1.72

Figure 12. Current difference of two modules plotted across different loading conditions.

The thermal shot shown in Figure 13 demonstrates two modules operating at 4kW without baseplate. The thermal performance shows a similar profile across the board with a single-digit temperature delta from its respective area.

Based on the key performance metrics presented, the ADI QBM reference design delivers a simple, robust, and highly competitive solution for customers seeking top-tier performance in high-power IBC applications within a CFP.



Conclusion

Legacy data centers face increasing challenges in meeting the growing demand for high-performance computing, driven by rapid advancements in AI and machine learning. Presently, DC architecture is adopting higher power density solutions on the system, utilizing 48V and 54V bus voltages to significantly reduce power losses compared to traditional 12V systems. A critical component in this transition is the IBC, particularly the QB power supply. These compact, efficient DC-to-DC converters play a critical role in converting HV DC input to lower voltages required by processors and peripheral systems.

With the rapid growth of AI, can 48V/54V architecture continue to meet the market's escalating power demands? Explore the latest solutions from ADI designed to answer this critical question.

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Karl Audison Cabas is an applications engineer focusing on power applications at Analog Devices since September 2020. He holds a bachelor's degree in electronics engineering from Polytechnic University of the Philippines and a postgraduate diploma in power electronics from Mapua University. He has more than 4 years of experience in DC-to-DC power converters. His previous function involved catering to customer inquiries and design issues related to DC-to-DC converters. He now works as a power system applications engineer for cloud and data center applications.

Christian Cruz is a staff applications development engineer at Analog Devices Philippines. He holds a bachelor's degree in electronics engineering from the University of the East in Manila, Philippines. He has more than 12 years of engineering experience in the field of analog and digital design, firmware design, and power electronics, which includes power management IC development as well as AC-to-DC and DC-to-DC power conversion. He joined ADI in 2020 and is currently supporting power management requirements for cloud-based computing and system communications applications.

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