ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Highly Integrated Multibeam Beamformers Offer SWaP Benefits for Payload Phased Array Antennas

Qui Luu, Senior Manager, and
John Wise, Former Catalog Modules Manager

Abstract

The appetite for high data rate and ubiquitous terrestrial connectivity has stimulated huge investment in low Earth orbit (LEO) constellation systems. Low orbit significantly reduces launch and equipment costs, cuts latency by 20× compared with GEO links, and manages bandwidth and users more efficiently. LEO satcom services promise worldwide coverage on the ground, at sea, and in-flight, reaching rural and remote regions, as well as supporting disaster zones where ground-based networks might be disabled. For this vision to be realized, electronically steered arrays at both ends of the link become essential to support the continuous, independent, fast scanning of multiple beams and the regular hand-offs as satellites come in and out of view. The payload is particularly challenging because it operates in a power-limited environment when DC power dissipation is critical. In addition, a high level of functionality such as multibeam capability, beam-hopping, beam memory, and the ability to scale the number of beams to support any mission requirement. Analog Devices has designed and productized a family of multibeam beamforming ICs that support payload beamforming applications with low power, high level of functionality and can scale with mission requirements.

Introduction

Most common satellite communications were originally based on geostationary satellites (GEO) where only three satellites were required for global coverage. These are large satellites (>1000 kg) where typically a single satellite would be on a launch vehicle. While this type of deployment was beneficial for broadcast applications such as television and radio, there were limitations. One is the latency involved in communications simply by the great distance between the user and the satellite. Typical GEO orbits are near 36,000 km, which has an approximate end-to-end latency of 400 ms, approximately 10× higher than point-to-point fiber optics connections in the United States.[1] Secondly, while the GEO satellite covers much of the Earth, it cannot effectively cover the northern or southern poles of the Earth. As an example, Inmarsat's Global Xpress GEO satellites cover approximately ±75° off the equator.[2]

To create true global coverage, smaller (<500 kg) low Earth orbiting (LEO) satellites are being deployed with inclined orbits to cover both major and rural population areas and polar orbits to cover the poles. These constellations vary from several hundred to several thousand satellites. All of these require beamforming antennas since they are traveling around the Earth at 27,000 km/h at 600 km to 1200 km orbit altitudes. This translates to the end-to-end latency reducing to approximately 50 ms. Many satellites are in a single launch vehicle for each deployment, so the size and weight of these LEO satellites are critical. In addition, these satellites were developed to provide high speed data to the user so using the proper frequency plan is important. Traditionally, Ku band (10.7 GHz to 12.7 GHz downlink/13.75 GHz to 14.5 GHz uplink) had been used. However, there is a drive to higher frequencies that have wider bandwidths and can support higher data rates. K/Ka band is being actively leveraged (17.7 GHz to 21.2 GHz downlink/27.5 GHz to 31.5 GHz uplink) and many are investigating Q/V bands as the next frequency band (37.5 GHz to 42.5 GHz downlink/47.2 GHz to 51.4 GHz uplink).

These higher frequencies pose new challenges in the design and realization of a payload phased array antenna. As the frequency increases, the lattice pitch of the antenna elements decreases, minimizing the available board space. Traditionally, a discrete approach may have been possible using transmission lines for time delays, beam steering using phase shifters/digital step attenuators or vector modulators, and embedding the Wilkinson splitters/combiners in the printed circuit board (PCB) itself. However, at these higher frequency bands, the PCB area is a significant challenge, which is driving the need for higher integration for ease of design and manufacturability. Additionally, the need for multibeam arrays drives additional complexity.

Beamforming ICs define electronically steerable phased arrays (ESA) and serve as the most critical building block. Interwoven in between the beamforming ICs are a power combiner and splitters, which distribute the signals to every beamforming IC. It is the combination of the beamforming IC, power combiner/splitter, and the fabric that weaves these two components together in a PCB design that determines the performance of the ESA.

Beamforming Integrated Chip

To maximize data rate, high throughput satellites (HTS) use multiple spot beams to distribute data effectively. Typical payloads in HTS satellites use multiple beams, which can be steered and hopped to maximize spatial and frequency reuse. Beam steering is accomplished by changing the phase of the beam as well as the amplitude at each element of the phased array antenna. To determine the number of variable amplitude and phase (VAP) devices that are required, multiply the number of beams for the satellite by the number of elements for the antenna and the product is the required number of VAPs.

As an example, for a configuration of 576 elements and 16 beams, the number of VAPS is 9,216 per array. If one considers using a discrete vector modulator as the VAP, which typically is 3 mm × 3 mm and consumes approximately 0.5 W, which will yield a dimension of 0.27 m × 0.27 m consuming over 4 kW of DC power. To put this into perspective, a 576 element array at 30 GHz with half wavelength spacing is 0.113 m × 0.113 m. As this illustrates, a higher level of integration is required for higher frequency phased array payload solutions, as well as a solution with minimal power consumption.

A unique approach to solving this problem was taken by Analog Devices in the design of the ADAR3000 and ADAR3001. These beamforming ICs are targeted for K/Ka band satellite payload applications. These devices are a 4-beam/4-element configuration that includes 16 VAP channels. The size of the resultant beamformer is 7 mm × 12.5 mm, which is a fraction of the array size if using a vector modulator approach. Additionally, to drive down power consumption, the VAP channels use passive structures. In the case of the ADAR3000/ADAR3001, the VAP is constructed of a digital step attenuator (DSA) and digital time delay unit. This design creates a 4-beam/16-channel beamformer that draws less than 200 mW of DC power. Figure 1 shows a block diagram. These devices are designed on a semiconductor process that supports space missions and can be used for LEO/MEO/GEO applications. The beamformers have passed radiation levels of 100 krad TID and 80 MeV SEE.

Scalability

Not all payload antennas are solely 4-beam designs. Higher beam count is required based on the constellation and mission. Beam count is often in multiples of 4 so being able to scale a solution from 4 beams to 8, 16, or 32 beams is critical. ADI's beamformers can easily be scaled to address higher beam count as well as varying element count. See Figure 2 for an example of a 16 beam/16 element array.

Figure 2 leverages a blade construction where each blade consists of 4-beam beamforming ICs. For this example, we will look at the transmit antenna, but one can reverse this to support the receive antenna using the appropriate receive beamforming IC. Each blade supports 4 elements. To support 16 elements, 4 blades are needed. Each beam needs to be present at each blade so each beam needs to be split 4 ways and then routed to each blade. Beams 0 to 3 then drive one of the beamforming ICs, beams 4 to 7 the second, beams 8 to 11, and lastly beams 12 to 15 driving the fourth beamforming IC. The output of each beamforming IC represents elements 0 to 3 on the array with each

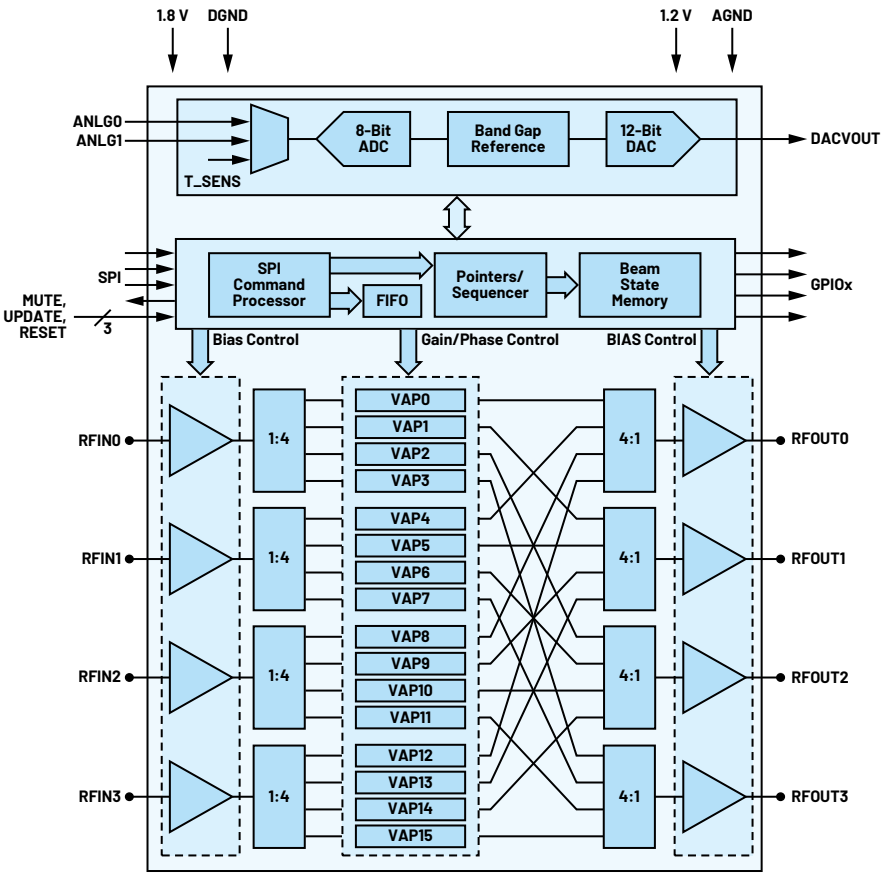

Figure 1. ADAR3000/ADAR3001 block diagram.

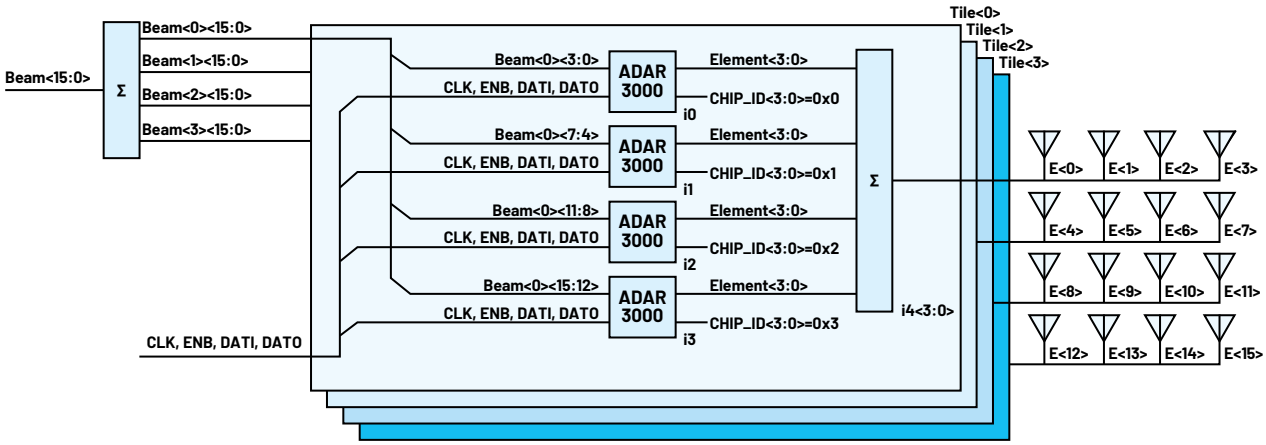

Figure 2. Scalability of the ADAR3000/ADAR3001 for higher beam count. Note that the PA and filter are not shown at the element.

beamformer weighting each beam appropriately for the given position of the element in the array. Since each ADAR3000 is outputting the beams for elements 0 to 3, the outputs then need to be combined to ensure all 16 beams are present at each element. The same is true for elements 1, 2, and 3. Before driving the elements the designer should select the appropriate power amplifier (PA) to support the antenna's EIRP and tapering requirements.

This construction can easily scale to support more or fewer beams and elements. Increasing the number of tiles will easily support more elements. Adding or reducing the number of beamforming ICs allows the designer to adjust to the number of beams required.

Digital Feature Set

In addition to size and power, digital control and functionality are important in the effort to minimize size, weight, and power (SWaP) in the payload. Requirements such as beam hopping need to be performed easily and quickly. To support beam control as close to the elements as possible, a sophisticated digital section is integrated into the beamformer IC. It is worth noting that each device has 4 address lines, so a single SPI bus can communicate with up to 16 beamformers, which minimizes the number of SPI lines and simplifies the array design. Each beam is independently controlled and has its own memory.

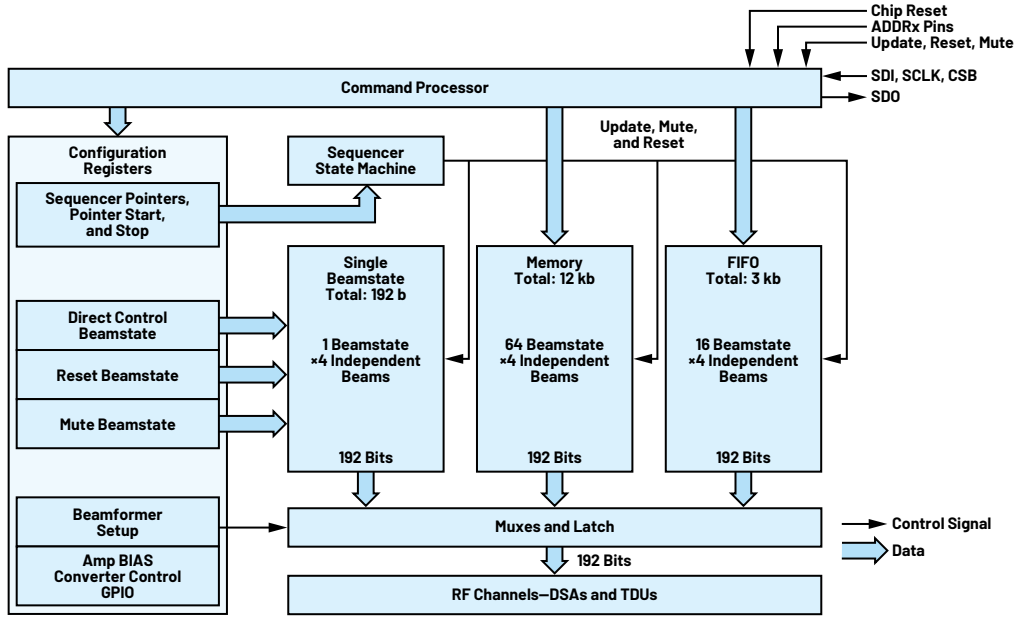

Figure 3. ADAR3000/ADAR3001 digital feature set.

The RAM and FIFO have their sequencer state machines that increment through the beam states that are stored within (see Figure 3). The RAM can store up to 64 beam states and the FIFO can store up to 16 beam states.

These features help support beam hopping and raster scanning of the antenna. When using the RAM with the sequencer, 64 beam states per beam can be programmed. Using the sequencer, the beam states can then be loaded in any prescribed sequence that is required. Similarly, in using the FIFO, once the beam states are loaded, the beam states can then be loaded in FIFO order.

Note that when using the internal memory, beam updates are very fast. Single VAP response time is < 10 ns. Update-to-update minimum timing is < 50 ns.

Wilkinson Splitter/Combiner

As previously mentioned, the beamformer IC's design and higher levels of integration within a package offer substantial SWaP advantages. Likewise, the design decision of the power combiner/splitter interlaced between the beamformer ICs needs to be optimized for SWaP trade-offs. Since the power combiner/splitters face the same design challenges, as in minimal PCB area due to tight lattice spacing constraints, small size, and optimized PCB routing are key for system performance and signal integrity.

First and foremost, the power combiner/splitter for phased arrays is passive. Thermal management for an active phased array is a difficult engineering challenge given the very small size and form factor and the high power handling capabilities. For this reason, the combiner/splitter is passive in order not to further burden the thermal requirements of the phased array.

Important performance characteristics to consider for combiners/splitters are frequency bandwidth coverage, port matching, isolation, minimal parasitic losses, and power handling. Achieving matched ports maintains symmetry where the input power splits evenly across all output ports and the phase difference between the output ports is kept to a minimum. Additionally, the input and output ports maintain a well-defined characteristic impedance.

The most common power combiner/splitter architecture used in phased array systems is the Wilkinson design. When all the ports are well matched, the Wilkinson divider offers the benefits of minimal loss, achieves high isolation between output ports, and is reciprocal. Wilkinson designs are commonly implemented directly on the PCB with microstrip and/or stripline. Alternatively, for improved SWaP benefits, monolithic silicon-based Wilkinson designs like the ADAR5000 and ADAR5001 prove quite advantageous in conserving PCB area, ease of routing, and improved signal integrity.

The ADAR5000 is a 1-to-4 Wilkinson power splitter that is designed for space-sensitive microwave signal distribution applications. Excess insertion loss ranges from −1.5 dB to −2.5 dB from 17 GHz to 32 GHz. The four outputs are matched in both phase and amplitude, making this device ideal for signal distribution applications requiring low time skew between channels. It can also be used as a combiner. The IC is housed in a compact, 2.5 mm × 2.5 mm × 0.5 mm WLCSP, which makes it ideal for use in planar, phased array antenna systems that require a tight pitch between elements. Similarly, the ADAR5001 is a 1-to-2 Wilkinson power splitter in a 1.5 mm × 1.5 mm × 0.5 mm WLCSP package.

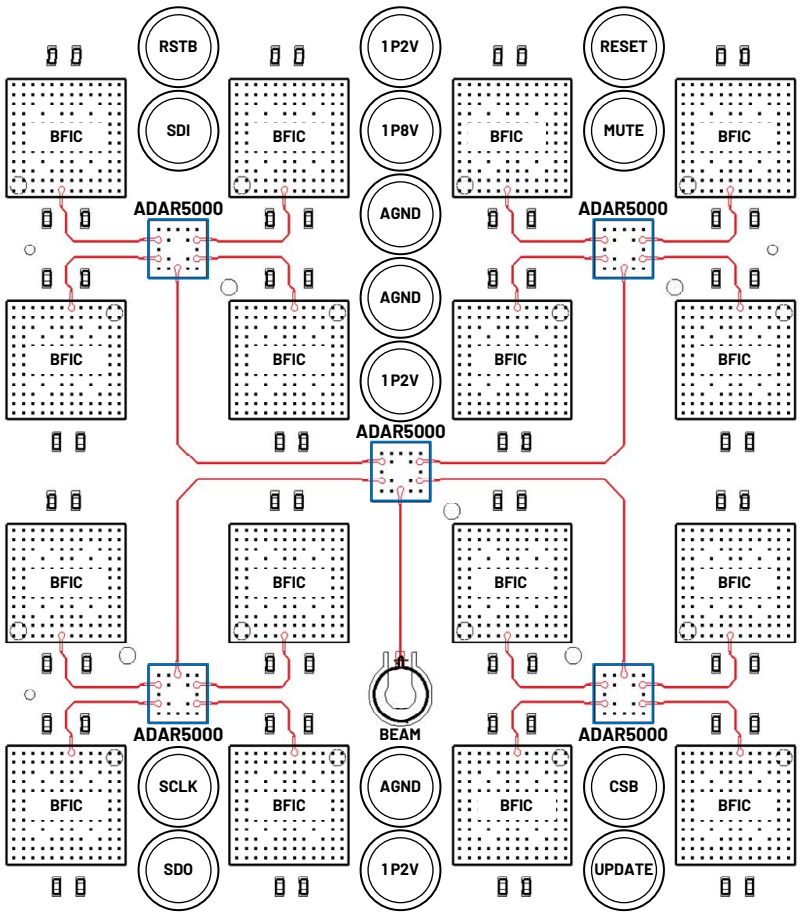

Figure 4. Beamforming IC with the ADAR5000 layout.

The ADAR5000/ADAR5001 offer substantial PCB area and cost savings over traditional Wilkinson power divider implementations utilizing a microstrip design on PCB. This is especially true at Ka band frequencies where the lattice spacing for a phased array design must be less than 5 mm at 31 GHz to prevent grating lobes. This lattice pitch must be shared between the beamforming IC and the combiner/splitters within an optimized layout structure. For example, for airborne satcom terminals at Ka band where the form factor of the complete phased array system is planar or 2-dimensional, the patch antennas reside on one side of the PCB and the beamforming IC and Wilkinson power dividers share the opposite side of the same PCB. Figure 4 shows the routing of a Ka band beamforming IC laid out in conjunction with the ADAR5000 1:4 splitter for applications requiring a 2-dimensional planar design. The layout is optimized and efficient where the high frequency traces are localized to the surface layer and the traces are direct, matched, and the shortest path from the device to the beamforming IC. Isolating the high frequency traces to the surface layer of the PCB allows for more controlled impedances of the traces and minimizes parasitic losses.

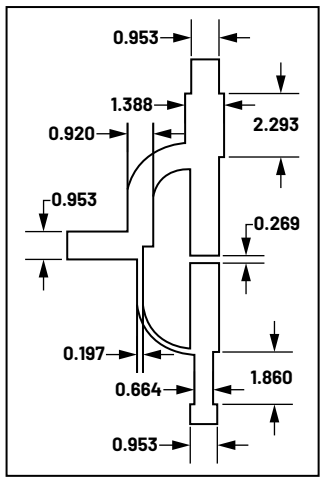

Figure 5. PCB microstrip layout of the 1:2 modified Wilkinson power divider. Dimensions in mm.[3]

The ADAR5000/ADAR5001 replace the traditional microstrip on PCB Wilkinson power divider designs. A microstrip design at Ka band requires substantially more PCB area. Figure 5 shows the layout of a 1:2 microstrip modified Wilkinson power divider on a Rogers' substrate at K and Ka bands.[3] Figure 6 shows the required footprint for the ADAR5001, which is substantially smaller in PCB area than the microstrip design. The footprint of the 1-to-2 Wilkinson power divider is in a 1.5 mm × 1.5 mm package and the 1-to-4, is in a 2.5 mm × 2.5 mm package. Only the form factor fits within the lattice spacing for Ka band frequencies up to 31 GHz.

Additionally, the performance of the Wilkinson power divider design is heavily dependent on the matching of the ports. The matching of the ports can only be as good as the tolerances of the manufacturing process of the PCB. Silicon tolerances are tighter and allow for smaller geometries.

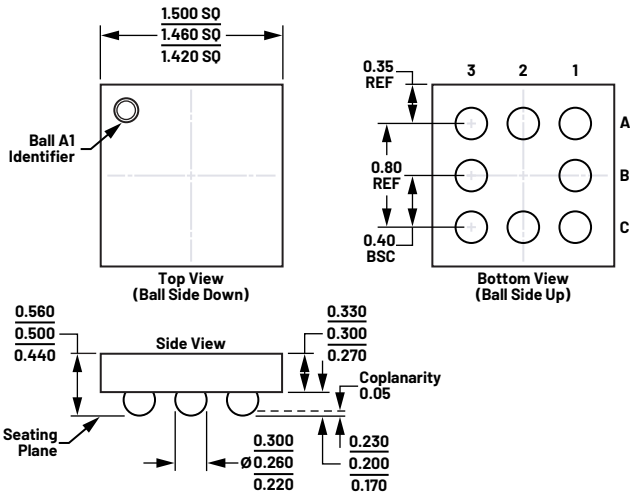

Figure 6. PCB footprint requirement for the ADAR5001, 1:2 Wilkinson power divider. Dimensions in mm.

Time Delay

To further improve and facilitate the system design of a phased array utilizing a corporate feed network, the ADAR4002 provides extended time delay and amplitude control in a single channel, low power, and miniaturized package. Given these features, it is an ideal component to distribute in a design to add slight adjustments in delay due to mismatches or to add additional delay compensation as needed for a true time delay phased array where the delay is inefficient to cover the bandwidth.

The ADAR4002 is a low power broadband, bidirectional, single-channel, true-time delay unit (TDU) and a DSA. The frequency coverage of the device extends from 500 MHz to 19 GHz with 50 Ω input impedance at both RF ports. The TDU has two programmable maximum time delays, each with a 7-bit control. Range 0 has a maximum delay of 508 ps with a resolution of 4 ps. For low frequency operation, Range 0 would be selected since more time delay is available for a full 360° phase coverage. Range 1 has a maximum delay of 254 ps and a resolution of 2 ps. This range has less insertion loss compared to Range 0 and is more suited for high frequency operation since the delay range is narrow with finer controls of the step size. The DSA has a 6-bit resolution with an attenuation range of 0 dB to 31.5 dB and a step size of 0.5 dB (see Figure 7).

Regarding the SWaP advantages of the ADAR4002, the power savings is quite substantial since the core building blocks of the device are passive. The TDU and DSA are passive while the digital is the only block that consumes power. With this said, this device is designed to provide flexible digital control through either a serial port interface (SPI) or a shift register. The shift register allows for daisy chaining of multiple chips. The IC contains register memory for 32 TDU and DSA states. The

memory combined with on-chip sequencers allows for fast bidirectional memory advancement via the UPDATE pin. These digital features prove advantageous for ease of use and fast beam hopping. The ADAR4002 consumes a total of 1 mW with 1.2 V and 1.0 V dual supplies.

The ADAR4002 is packaged in a 2 mm × 3 mm LFCSP package. The time delay range available in such a small package is quite amazing given all the potential use cases for this component. It can be placed strategically in a design to compensate for PCB length or delay tuning. For very large phased arrays, it is difficult to length match all the signal traces on the PCB. For this reason, delay tuning may be required. The goal is to set the lengths of signal traces in a matched group of nets to the same length value. This ensures all signals arrive within some constrained timing mismatch. The most common approach to achieving synchronization of the signal traces is to add delay to the shorter signal trace by adding some trace meandering such as trombone, sawtooth, or accordion. Trace meandering comes at the expense of PCB area and design time since a unique trace is required for a specific time delay. To put this into perspective, for a high frequency board material such as Isola Astra MT77 or Rogers 3003, where the dielectric constant is 3.0, approximately 3.5 inches of stripline or 4 inches of microstrip is required to achieve 508 ps of delay. Table 1 shows the propagation delay for a few PCB materials as collected by the Sierra Circuits Team.[4] The PCB area required is quite substantial compared to the small 2 mm × 3 mm package of the ADAR4002, which offers a range of delays in a single footprint.

Table 1. Propagation Delay for a Few PCB Materials[4]

Material	Er	Er_{eff}	V Microstrip	V Stripline	t_{pd} Microstrip	t_{pd} Stripline
Vacuum or Air	1	1	11.8 in/ns	11.8 in/ns	85 ps/in	
Isola 370HR	4.0	2.92	6.90 in/ns	5.9 in/ns	145 ps/in	170 ps/in
Isola I-Speed	3.64	2.69	7.20 in/ns	6.18 in/ns	139 ps/in	162 ps/in
Isola I-Meta	3.45	2.57	7.36 in/ns	6.35 in/ns	136 ps/in	158 ps/in
Isola Astra MT77 or Tachyon 100G or Rogers 3003	3.0	2.28	7.8 in/ns	6.8 in/ns	128 ps/in	147 ps/in
Rogers 4000 Series	3.55 – 3.66	2.63 – 2.7	~7.20 in/ns	~6.20 in/ns	~139 ps/in	~161 ps/in

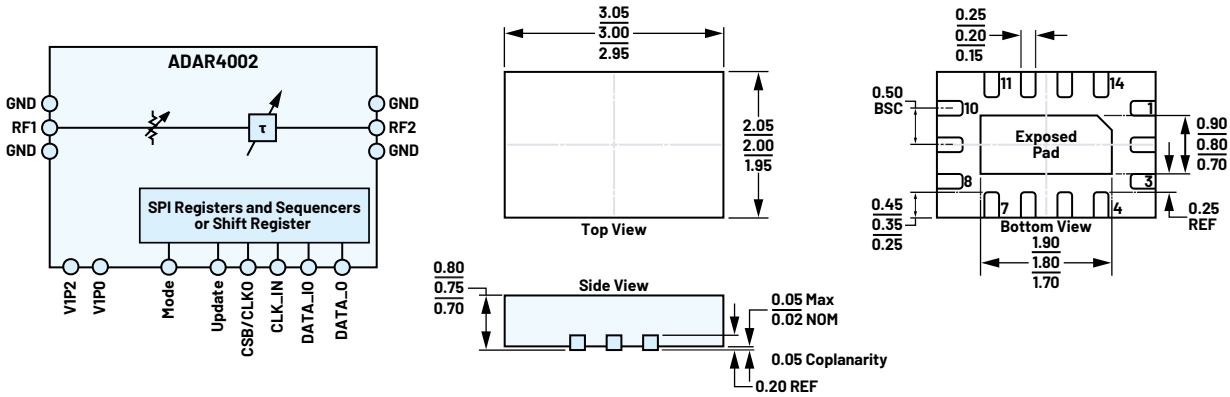

Figure 7. ADAR4002 block diagram and package outline. A 14-lead lead frame chip scale package (LFCSP) 3 mm × 2 mm body and 0.75 mm package height (CP-14-6). Dimensions are shown in mm.

Conclusion

Traditional discrete approaches to the design of phased array antennas for satellite payloads are not optimized for size, weight, or power. GEO satellites are large satellites where a single satellite resides on a launch vehicle. By contrast, today's LEO constellations require deploying many satellites on a single launch vehicle, which limits their size and weight. In addition, the demand for higher data throughput is pushing satellite communication frequencies from Ku band to K/Ka band and higher, requiring even smaller antenna arrays. Advances in silicon-based ICs have added higher levels of integration, functionality, and lower DC power consumption, which make for smaller, thinner, and lighter antenna apertures to support Ku band frequencies and higher to address the SWaP challenges of today's satellites.

References

[1] Yongguan Zhang, Dante De Lucia, Bo Ryu, and Son K. Dao. "Satellite Communications in the Global Internet: Issues, Pitfalls, and Potential." Hughes Research Laboratories, January 2016.

[2] Inmarsat Global Xpress Coverage Map.

[3] Dimitrios Antsos, Robert Crist, and L. Sukamto. "A Novel Wilkinson Power Divider with Predictable Performance at K and Ka-band." *IEEE MTT-S Digest*, 1994.

[4] Mohamed Faheemuddin. "What Is Signal Propagation Delay in a PCB?" Sierra Circuits, October 2023.

About the Authors

Qui Luu received her B.S.E.E degree from Worcester Polytechnic Institute, Worcester, MA, USA, in 2000. In 2005, she received her M.S.E.E degree from Northeastern University, Boston, MA, USA. Since 2000, she has been with Analog Devices, Inc., where she is currently a system engineer/IC architect in the Aerospace and Defense Organization located in Chelmsford, MA. Her focus area as of recent has been on beamforming ICs and system development from the antenna to bits for electronically steerable phased arrays.

John Wise received his B.S.E.E. degree from the Illinois Institute of Technology. Before retiring, he was the product line manager for beamforming ICs and SiPs in Analog Devices Aerospace and Defense organization. Prior to joining ADI, Mr. Wise held positions at Hewlett-Packard (now Keysight) and Hittite Microwave. He has over 30 years of experience in the design, development, and production of microwave and fiberoptic test equipment, components, modules, and custom assemblies and ICs for commercial, military, and hi-rel applications.